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AFCRL-62-375

ATC LINAR RECEIVER

by

W. F. Fickenscher

THE BENDIX CORPORATION
BENDIX RADIO DIVISION
BALTIMORE 4, MARYLAND

Contract No. AF19(604)-8848

Project No. 4655

Task No. 46550

FINAL REPORT

30 May 1962

Prepared
for

ELECTRONICS RESEARCH DIRECTORATE
AIR FORCE CAMBRIDGE RESEARCH LABORATORIES
OFFICE OF AEROSPACE RESEARCH
UNITED STATES AIR FORCE
BEDFORD, MASSACHUSETTS

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FOREWORD

This report is the final report and covers the work done at Bendix Radio under contract AF19(604)-8848 for The Electronics Systems Division, Air Force Systems Command (Laurence G. Hanscom Field, Bedford, Massachusetts). This report discusses the work done during the last period and the instructions for operating the finalized ATC LINAR Receiver.

ABSTRACT

The purpose of the program was to produce a LINAR receiver which will be compatible to the MPN-11 radar system. The program commenced on 10 July 1961 and was completed on 30 May 1962. A prototype model was built and tested and from these tests a final model was built and has been delivered to ESD (ESSVM). In producing the final model a few problem areas were encountered that are discussed in section 2. It was also necessary to make several trips to Hanscom AFB to make the system compatible to the MPN-11 radar system. A description of the final receiver is discussed in the last section of this report to present to the reader a description of the final model and how to operate this final receiver.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1. INTRODUCTION

The basic problems encountered in ground control approach radar systems are visibility in clutter areas and visibility during weather. The standard tools with which the operator can combat these problems are MTI (Moving Target Indicator Receiver), STC (Sensitivity Time Control), FTC (Fast Time Constant), and a manual gain control. Each has definite limitations on its usefulness. MTI exhibits blind speeds and is difficult to keep in proper adjustment. Both STC and gain control reduce the amplitude of targets as well as undesired signals. The use of a fast time constant circuit reduces the width of clutter signals, but sensitivity to targets is retained only when clutter amplitude is small (below limiting in the final IF stages and detector). Consequently, only when gain is reduced does it improve target visibility.

The Bendix LINAR receiver produces an output containing most of the good features of all the above operations, and it was the purpose of this contract to adapt such a receiver to the MPN-11. The ATC LINAR achieves extremely high sub-clutter visibility without the problem of blind speeds. This is done with a wide dynamic range linear detector followed by differentiation.

While the clutter is not entirely removed, as is the case in an MTI receiver, maximum sensitivity is retained to signals atop it. In addition, all clutter pulses of a longer duration than a target are rejected through pulse width discrimination. This leaves a residue of spikes from clutter on the indicator, but it is not sufficient to interfere with tracking.

Where in the case of the standard FTC, targets were visible only when gain was reduced to a level where the clutter was not limited, the LINAR receiver FTC requires no gain reduction because the detector does not limit. This means that targets are tracked at maximum sensitivity whether they are in the clear or in clutter.

Against weather the only useful device in the standard system is the gain control. By reducing sensitivity the operator may be able to track targets. With the LINAR, no manual gain control adjustment is necessary to optimize on targets in weather. That is, the receiver video gain changes to prevent indicator saturation. Any target that is larger than the noise component of the weather return will be presented.

The LINAR adds somewhat to the capabilities of the system. However, its primary advantage is that it simplifies the system operation. It allows the operator to track as well with no adjustment of controls as he formerly could by varying gain, etc. It allows tracking of several targets simultaneously with maximum sensitivity for each. Also, maintenance should be kept to a minimum since the device is completely transistorized.

2. DISCUSSION OF WORK DONE

2.1 PURPOSE

The purpose of the program was to develop a LINAR receiver which was compatible with the MPN-11 precision radar system. The primary objectives were to provide sub-clutter visibility, weather rejection, and high resolution. A prototype was built and tested during the last quarter and a final model was built and delivered to AFCS in May 1962. (See Figure 1.)

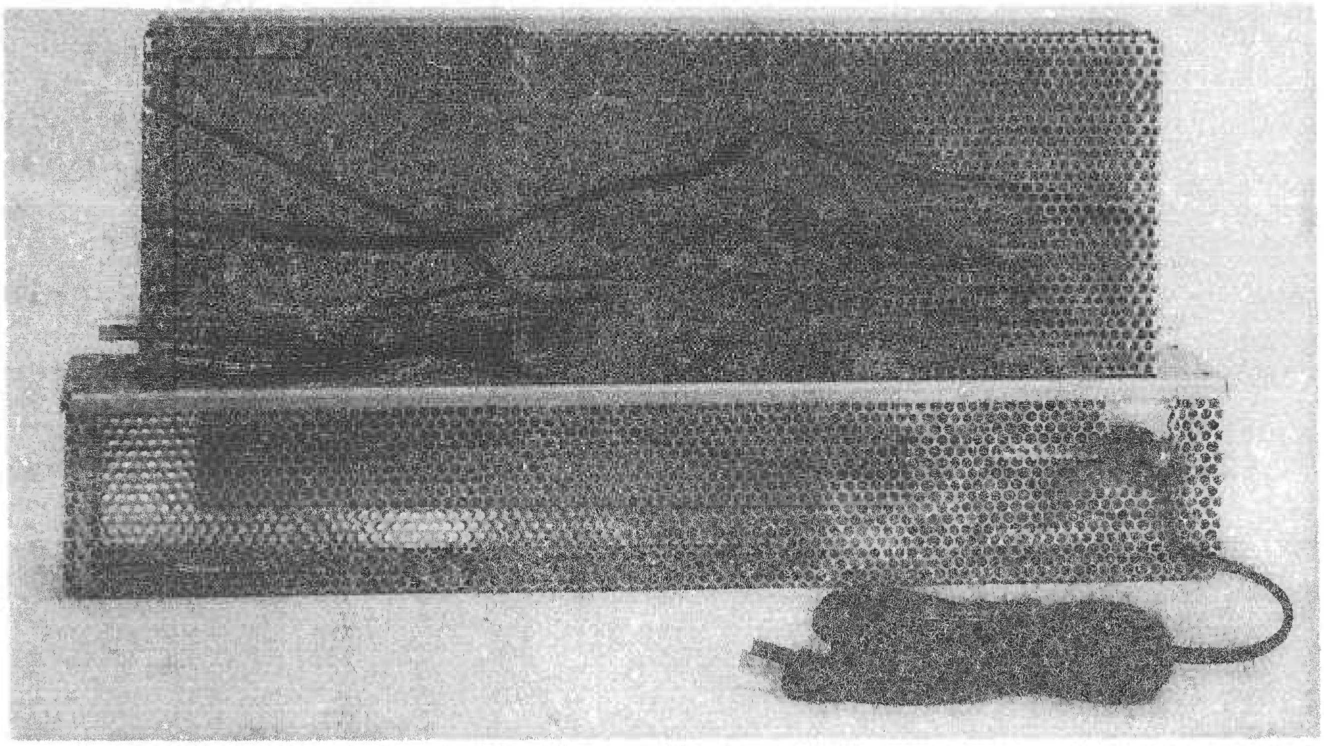


Figure 1. ATC LINAR Receiver

2.2 MAJOR PROBLEMS AND SOLUTIONS

The major difficulties encountered in adapting the Bendix LINAR receiver to air traffic control use were in wide-banding the basic circuits. The original LINAR receiver design was for narrow bandwidth search radars and

it was necessary to improve the response considerably, particularly of the integrators which are used in the signal line.

Another problem was the necessity of producing an extremely fast differentiation without an appreciable loss of sensitivity. This was achieved with a series R-L-C circuit. After a leading or trailing edge of a signal, the FTC returns to the base line in approximately twice the pulse rise time.

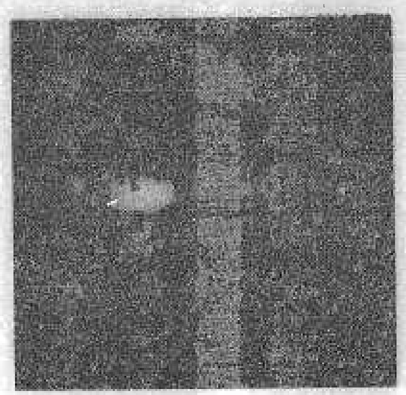
The original design called for a single detector with a wide dynamic range. After some testing it was determined that optimum operation of the receiver demanded a truely linear detector with a wide dynamic range. The Bendix linear receiver (O. H. Baust, 15 March 1960, T-11, 229-5) was such a device. The idea of several parallel detectors was incorporated into the LINAR, and the IF and detector circuits, were designed and tested.

A further problem was encountered in the 30-MC leakage through the detector stages after they became saturated. For linear detector action this is not tolerable. A filter was added to each detector consisting of a toroid and a capacitor. This afforded the proper bandwidth necessary for video while rejecting the undesired 30-MC signals.

The packaging of the receiver into the space occupied by the normal receiver was specified in the contract. The receiver was installed on the MPN-11 and was found to mount easily.

The receiver which has been developed is currently being tested and evaluated at AFCS headquarters, Scott AFB, Illinois. Section 3 of this report will deal with the operation and maintenance of the receiver itself in order to facilitate the testing and aid in evaluation. Photographs were taken at Hanscom AFB, Massachusetts showing the ability of the LINAR receiver. The first pair of pictures (Figure 2) shows the ability of the Bendix ATC LINAR to break up the clutter as compared to the normal receiver. In the succeeding pictures (Figures 3 and 4), which were taken over several indicator scans, the sensitivity of the LINAR is illustrated. The targets are readily tracked through

the clutter area. For all the multi-scan pictures, the gain control was set for maximum sensitivity and not adjusted.



SYSTEM NORMAL
RECEIVER
MPN-11

BENDIX LINAR
RECEIVER

Figure 2. Photographs of Single Scan

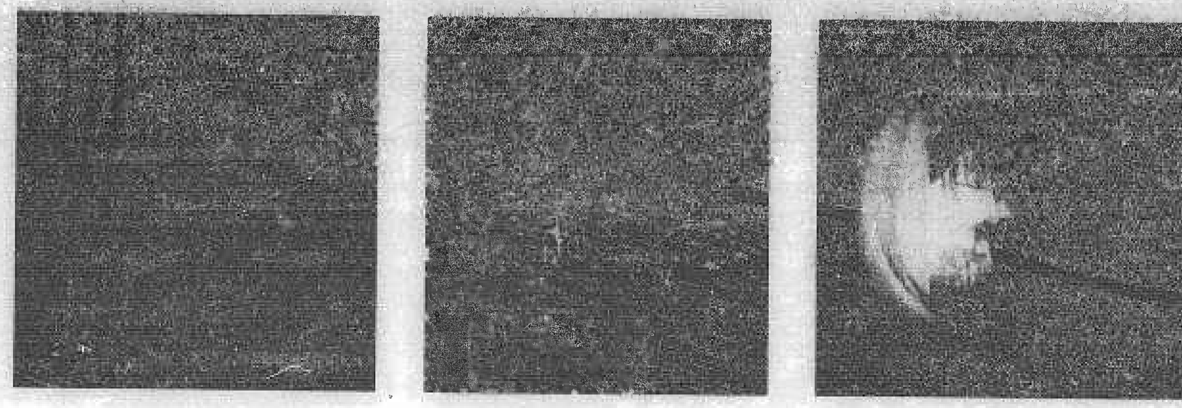
2.3 ADMINISTRATION

The work performed on this contract was under the direction of Mr. J. Martin. During the first quarter, the design engineer was Mr. O. Baust, and thereafter his duties were transferred to Mr. W. Fickenscher. The mechanical design work was done by Mr. J. Baker , Mr. J. Bode,and Mr. L. Bosse assisted the above group.

2.4 TRAVEL

Several trips were involved in producing the receiver. Early in the contract Mr. Baust and Mr. Baker made trips to Hanscom AFB to gather the necessary information for adapting the receiver to the MPN-11. During the last quarter Mr. Baust and Mr. Fickenscher performed tests with the prototype

at Hanscom, and later, Mr. Martin accompanied several others to oversee the acceptance testing of the final model.

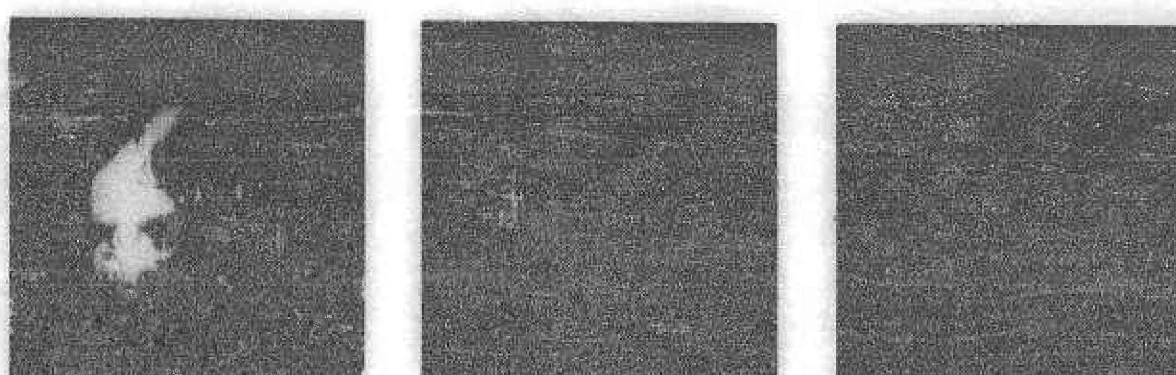


BENDIX LINAR RECEIVER (TARGET 5-7MILES) T-33

BENDIX LINAR RECEIVER (TARGET ON RUNWAY)

SYSTEM NORMAL RECEIVER MPN-11

Figure 3. Photographs of Multi-Scans with Target on Runway and 5-7 Miles Away



SYSTEM NORMAL RECEIVER MPN-11 (TARGET IN CLOSE)

BENDIX LINAR RECEIVER (TARGET IN CLOSE) T-33

BENDIX LINAR RECEIVER (TARGET IN CLOSE)

Figure 4. Photographs of Multi-Scans with Target in Close

3. DESCRIPTION OF FINAL EQUIPMENT

3.1 THEORY OF OPERATION

The Bendix ATC Receiver is designed to combat some of the major problems encountered in ATC radars. These include clutter, weather, and interferring radar returns.

Subclutter visibility is obtained by differentiation immediately after detection by a wide dynamic range linear detector. Clutter amplitude does not affect sensitivity to small targets as long as the dynamic range (approximately 60 DB) is not exceeded. Tracking is facilitated because the receiver removes the low frequency components of the clutter, allowing only the high frequency clutter fluctuations to pass. The remaining clutter profile is jagged and contains numerous holes. Due to the linear detector, targets are tracked through this residue at maximum sensitivity. Some of the remaining clutter spikes as well as improper length radar signals are rejected in a pulse width discrimination circuit.

Weather rejection is obtained with a video CFAR (constant false alarm rate) circuit which retains sensitivity to targets larger than the noise component of the weather. In addition to the above capabilities, the receiver contains a normal receiver output which can be used separately or simultaneously with the ATC LINAR output.

3.2 MECHANICAL INFORMATION

The Bendix LINAR Receiver is designed to replace the normal receiver on the MPN-11. It mounts in the same location as the old normal receiver. The unit is completely transistorized and contains its own power supplies. AC is applied through a connector near the bottom of the chassis. There are three coaxial cable connections. The input and the normal receiver output are the same as the existing normal receiver cables. The third is the ATC LINAR output which connects to the video switch chassis, paralleling the normal output.

3.3 ANALYSIS OF OPERATION

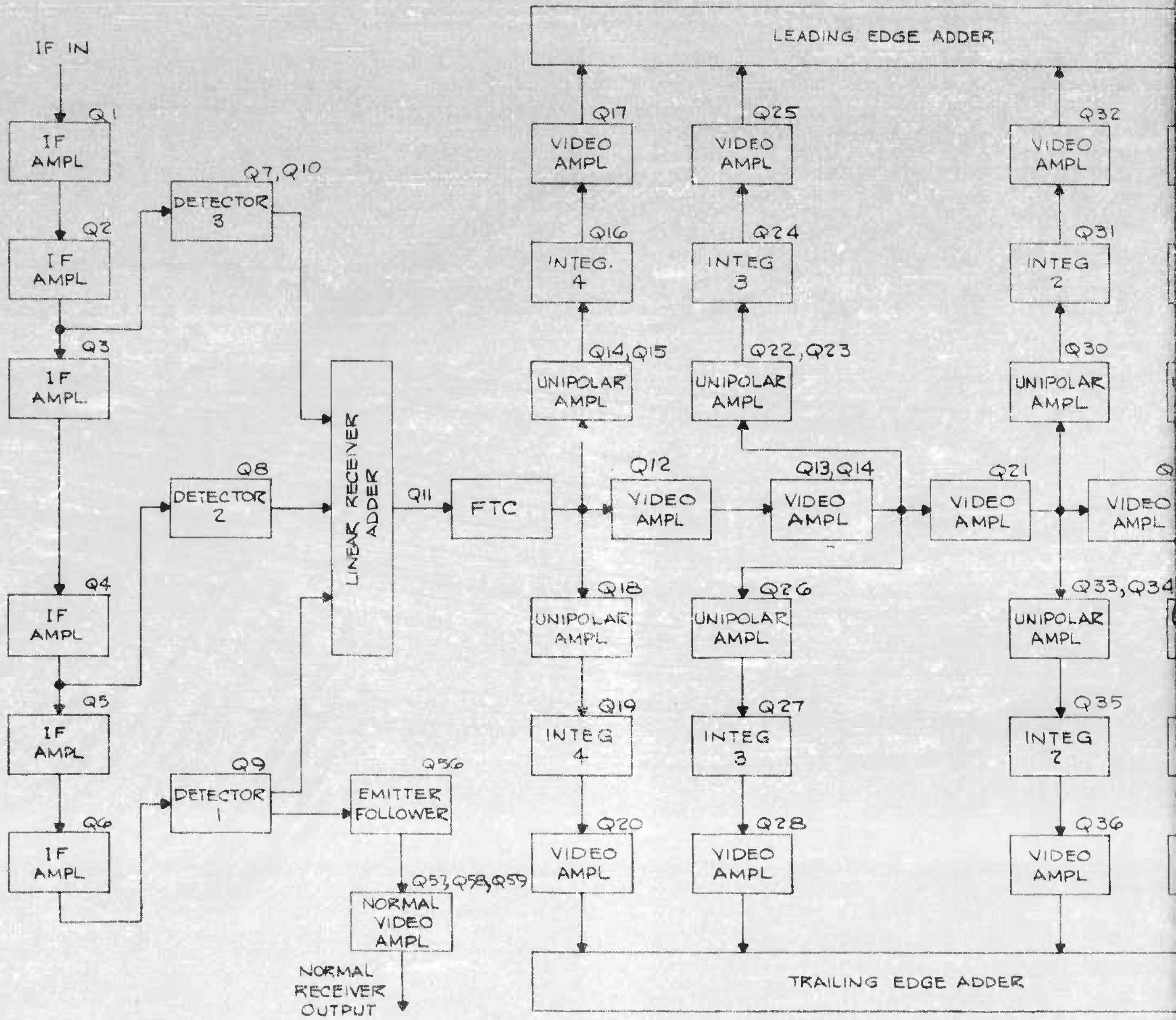
In the following description references will be made to the simplified block diagram, Figure 5, as well as the schematic diagram Figure 6. 30-MC signals from the preamplifier are applied to the first of six cascaded common base stages, Q1 through Q6. The bias circuits for these tuned stages include thermistors for temperature stability. For Figure 6 see back cover.

The output of the final IF stage (Q6) is transformer coupled to detector 1 (Q9). Detection occurs in Q9 when bias is adjusted for Class "B" operation. The bias control is R50. Associated with Q9 is a 30-MC trap for filtering and gain pot R52. The dynamic range of the detector is about 20 DB. That is, small signals are detected, but signals more than 20 DB above system noise level cause the stage to saturate.

For signals large enough to saturate detector 1, the level is great enough to be detected at the output of Q4 by detector 2, Q8. This stage is identical to detector 1, but its dynamic range covers signals over a 20-DB range which starts where that of detector 1 ends.

Similarly, detector 3 (Q7) takes over for still larger signals. The outputs of the three detectors are combined in a weighted adder circuit so that the gain to any signal is equal regardless of the path from the input to the linear receiver adder. To adjust the gain of the three channels so that linearity can be obtained, gain controls R52, R45, and R36 are located in channel 1, 2, and 3 respectively. The linear receiver adder utilizes the dynamic range of all three detector channels so that small signals and system noise remain essentially the same size regardless of the amplitude of the clutter pulses they ride upon.

From the adder, signals pass through another filter section and into an emitter follower (Q11) which drives the differentiator (FTC). Gain pot resistor (R57) sets the level for the video CFAR circuit which follows.


IF IN
Q1
IF AMPL
Q2
IF AMPL
Q3
IF AMPL
Q4
IF AMPL
Q5
IF AMPL
Q6
IF AMPL
Q7, Q10
DETECTOR 3
Q8
DETECTOR 2
Q9
DETECTOR 1
LINEAR RECEIVER ADDER
Q11
FTC
Q56
EMITTER FOLLOWER
Q57, Q58, Q59
NORMAL VIDEO AMPL
NORMAL RECEIVER OUTPUT
LEADING EDGE ADDER
Q17
VIDEO AMPL
Q16
INTEG. 4
Q14, Q15
UNIPOLAR AMPL
Q12
VIDEO AMPL
Q18
UNIPOLAR AMPL
Q19
INTEG 4
Q20
VIDEO AMPL
Q25
VIDEO AMPL
Q24
INTEG 3
Q22, Q23
UNIPOLAR AMPL
Q13, Q14
VIDEO AMPL
Q26
UNIPOLAR AMPL
Q27
INTEG 3
Q28
VIDEO AMPL
Q32
VIDEO AMPL
Q31
INTEG 2
Q30
UNIPOLAR AMPL
Q21
VIDEO AMPL
Q33, Q34
UNIPOLAR AMPL
Q35
INTEG 2
Q36
VIDEO AMPL
VIDEO AMPL
TRAILING EDGE ADDER

1

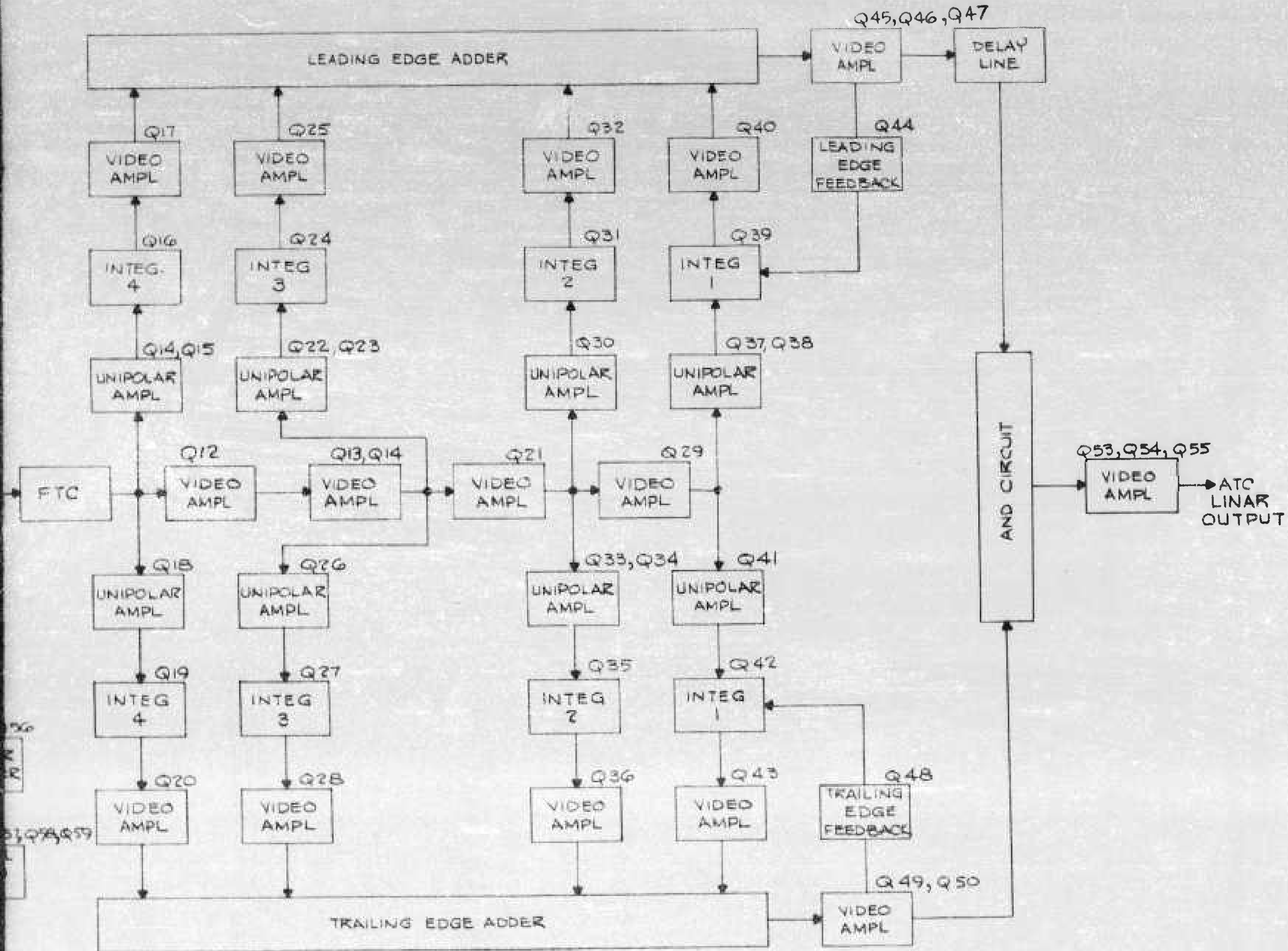


Figure 5. ATC LINAR Receiver, Block Diagram

2

The differentiator time constant is adjusted for rapid return to the base line after a large leading or trailing edge. At this point in the circuit, leading or trailing edges of all clutter spikes and signals will appear in linear relationship to their input amplitude. Effects of CW jamming have been removed by differentiation without loss of sensitivity to signals. Weather or noise jamming, however, will cause an increase of noise level that is directly proportional to the input amplitude.

The video CFAR (constant false alarm rate) circuitry is designed to remove fluctuations in the output noise level due to weather or noise jamming while retaining sensitivity to any signal larger than the noise. It consists of four cascaded video amplifier stages (Q13, Q14, Q21, and Q29) which drive various taps as shown in the block diagram. System noise and small signals are amplified through this chain. The output of the final stage (Q29) feeds two transistors, Q37 and Q41. Q37 is an inverter, and the remainder of the channel it feeds, Q38, Q39, and Q40, is identical to the other channel consisting of Q41, Q42, and Q43. Amplifiers Q38 and Q41 each clip off the positive portion of the input signals. For Q41, this means that only trailing edges of clutter and target pulses are passed, since signals at the linear receiver adder are positive. Due to inversion in Q37, Q38 clips off trailing edges but passes leading edges. The output of Q38 feeds emitter follower Q39, which in turn drives an integrator circuit consisting of CR13, C62, and several resistors. The integrator charges quite rapidly and discharges somewhat slower. It couples directly to the base of amplifier Q40. The receiver is adjusted so that system noise and small signals are integrated just enough to bias Q40 almost to cut-off. If the noise level increases, the integrator increases the bias and Q40 turns off.

As the noise level increases enough to cut off Q40, the amplitude at the base of Q32 in the next channel becomes large enough for it to produce an output. A further increase in noise level causes Q32 to be biased off and the

next channel to produce the output. The outputs of the four similar channels are combined in the leading edge adder. Gain in the channels is adjusted by means of the pot in the collector of each output transistor, R185, R147, R113, and R73.

In the case of the linear receiver adder, all signals received the same amount of gain regardless of the path they took from input to adder. At the leading edge adder, however, the signals receive less gain through channel 2 than through channel 1, less gain through channel 3 than through channel 2, etc. The result is that when the gains are properly adjusted, the noise level at the adder will remain constant as the noise level at the input increases. The operation of the four channels feeding the trailing edge adder is identical with the action on the leading edge side. The circuitry in each channel is identical with its leading edge counterpart, except that in each channel an inverter is necessary in one side or the other so that the proper polarity signal is picked off.

The output of each adder feeds a gain controlled emitter follower and an amplifier (Q45 and Q46 on the leading edge side, and Q49 and Q50 on the trailing edge). The output of Q46 feeds the base of Q44. This stage is biased off by adjustment of R206 and conducts only when a large signal appears at the collector of Q46. The collector of Q44 is connected to integrator 1, the base of Q40. The function of this feedback stage is to discharge the integrator quickly after a large pulse so that recovery time of the receiver is minimized. In the trailing edge side, Q48 performs the same function as Q44 in the leading edge side. The collector of Q50 also drives a fast time constant circuit (C82 and R227) which removes slow shifts in the base line from bursts of noise such as weather. Signals are then applied to the "AND" circuit driver Q51.

On the leading edge side, Q46 drives a similar fast time constant, C70 and R211. Signals are then applied to the delay line driver Q47. All signals on this side of the receiver represent the leading edge of a clutter or target pulse. The delay line delays these signals one transmitter pulse length so that for a true target, the leading edge and trailing edge arrive at the "AND" circuit simultaneously.

The "AND" circuit consists of diodes CR20 and CR24 and resistors R219, R236, and R237. When a signal is present at the input to CR20 but not at the input to CR24, CR20 is cut off; but bias current still flows through CR24. This causes only a slight variation in voltage across R237. The same result is obtained if a signal appears at the input to the trailing edge of diode CR24 but not at CR20. However, when signals occur at the two inputs simultaneously, as in the case of a proper target, all current through the diodes ceases and the voltage across R237 changes considerably. This results in a rejection of improper length signals since leading and trailing edges will not occur simultaneously.

The remainder of the circuit consists of emitter follower Q53, amplifier Q54, and an output driver Q55. R240 in the emitter of Q53 provides gain control for the output video. The bias on Q54 is variable (R242) to allow base line clipping when necessary and maximum signal-to-noise ratio is adjusted by varying the bias on limiter diode CR25 with R246. Aside from the several taps, the IF section of the receiver is the same as any linear IF amplifier. After detection by Q9, the output is that of a normal receiver. The normal video output circuitry consists of an isolation follower Q56, two amplifiers Q57 and Q58, and an output driver Q59. Gain control is provided by R260 in the collector of Q57 and maximum signal-to-noise ratio is set by varying the bias on limiter diode CR26 with R267.

3.4 ALIGNMENT PROCEDURE

3.4.1 Power Supply Adjustment

The power supply for this unit is located on the bottom of the chassis under the shelf. It should be adjusted before the unit is mounted. With DC voltmeter between negative terminal of C702 and ground, adjust R701 for -8 VDC. See Figure 7.

3.4.2 IF Alignment

The IF alignment shall be performed as follows:

1. Apply a 30-MC signal to the preamplifier input (or an RF pulse into the system in front of the crystal mixer).

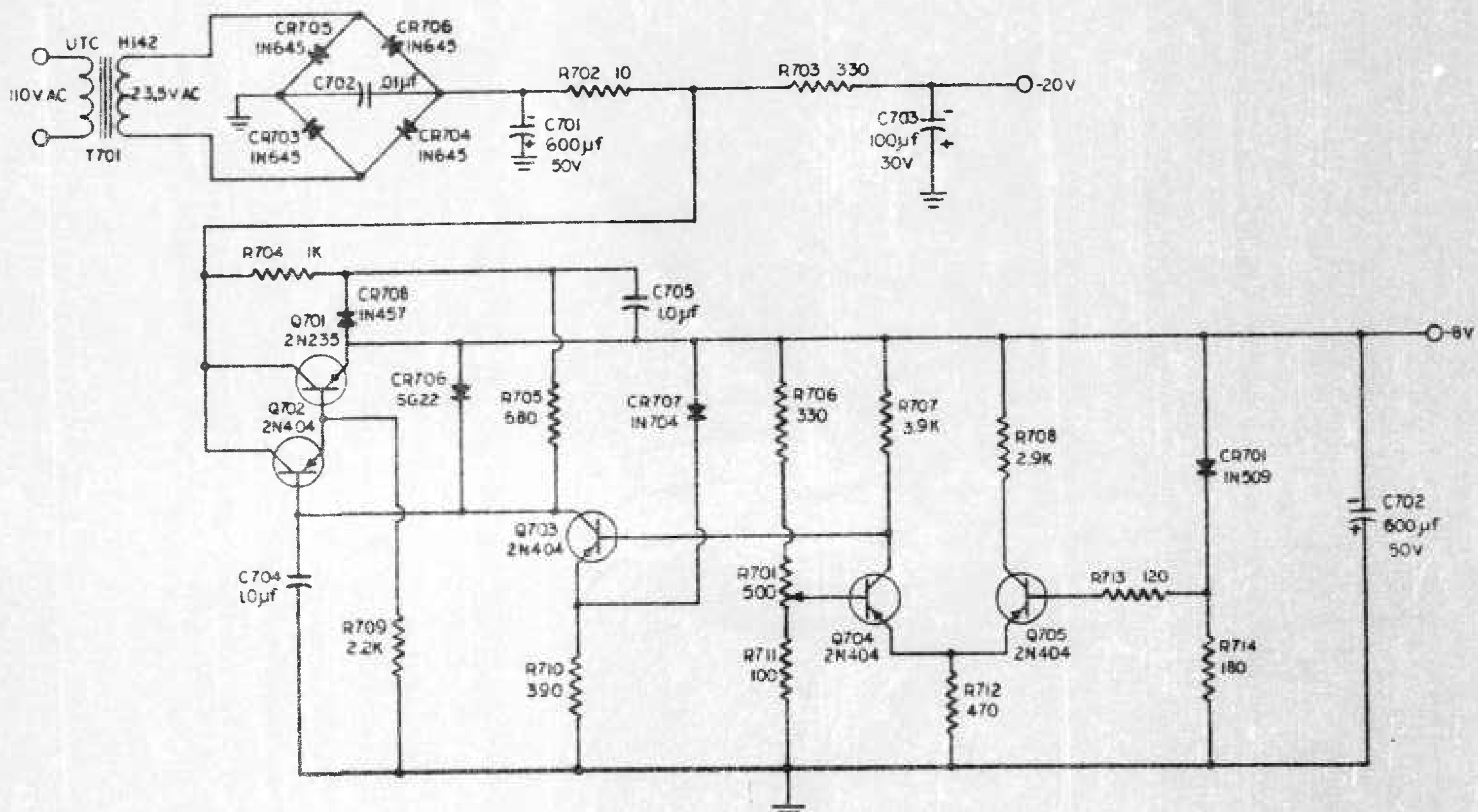


Figure 7. ATC LINAR Receiver Power Supply, Schematic

2. Connect signal cable from preamplifier to "IF IN" jack J1 of Bendix ATC LINAR Receiver.

3. Connect scope probe to collector of Q9. Tune T6, T5, T4, T3, T2, and T1 for maximum positive signal at this point.

3.4.3 Linear Detector Adjustment

Perform the linear detector adjustment as follows:

1. Set preamplifier gain slightly below maximum.

2. Set resistors R36, R38, R44, R45, and R50 to maximum counter-clockwise. Set R52 maximum clockwise.

3. With scope probe on collector of Q9, adjust R50 until noise just reaches maximum.

4. With scope probe on center arm (green lead) of R52, adjust R52 with approximately 0.3V peak noise.

5. Apply a signal as in step 1 of section 3.4.2 above. Adjust its amplitude to be about 50-60 DB larger than the smallest discernible signal at the collector of Q9.

6. Connect probe to base of Q37. Adjust R53 for fastest return to base line without overshoot after leading or trailing edge of the differentiated pulse.

7. Adjust R57 for approximately 0.2V peak-to-peak of noise at this point.

8. Apply a long pulse (10 or more microseconds in duration), as in step 1 of section 3.4.2 above. Vary the amplitude of the input signal. As the input amplitude increases, the noise level during the pulse will increase slightly and then drop off. At about 20 DB to 30 DB adjust R45 to bring it up equal to the level of the noise outside the pulse.

9. Increase the input about 20 DB further, and adjust R36 for constant level as in step 8.

10. The detector is linear when the noise level during a pulse remains constant over the entire range of input amplitude. By proper adjustment of the contribution from each detector, an essentially constant noise level can be obtained over a 60 DB range. If necessary, readjust resistors R52, R45, and R36.

11. Readjust R57 for approximately 0.2V peak-to-peak noise at base of Q37.

3.4.4 CFAR Video Adjustment

The CFAR video adjustment shall be performed as follows:

1. Set resistors R73, R96, R113, R128, R147, R164, R185, R200, R206, and R232 fully clockwise.
2. Set R211 and R227 fully counterclockwise.
3. With equipment as shown in Figure 8 (scope probe on base of Q37), adjust input noise level with the attenuator until a 3-DB change on the attenuator makes a barely discernible change in the noise at Q37.

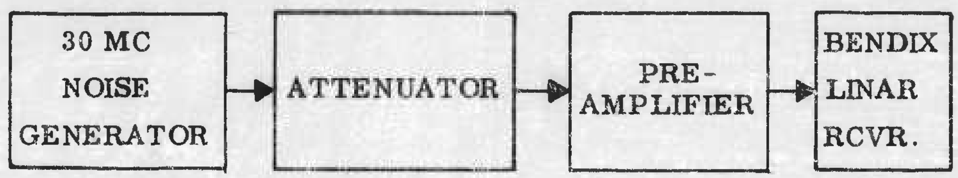


Figure 8. Test Setup for CFAR Video Adjustment

4. With scope probe on collector of Q46, adjust R250 for about 0.5V peak noise.
5. Scope probe on base of Q47. Vary the attenuator over a range of about 60 DB in 10-DB steps from the original setting (step 3). The noise level should remain essentially constant although the character or appearance of the noise may change. If the level does not remain constant, slight readjustment of R185, R147, R113, and R73 may be necessary.
6. Return to the original attenuator setting (step 3). With scope probe on collector of Q50, adjust R223 for about 0.5 volts peak noise.
7. Vary the attenuator over a 60-DB range from the original setting. The noise level should remain essentially constant. If it does not, slight readjustment of R200, R164, R128, and R96 may be necessary.
8. Remove noise generator from the input to the preamplifier. Apply a signal to the preamplifier. With scope probe on base of Q37, set the signal amplitude for the smallest discernible signal.
9. Increase the signal size by about 60 DB.
10. Scope probe on collector of Q46. Adjust R206 counterclockwise. Recovery time after the leading edge will decrease to about 1 microsecond. Beyond this point adjustment has no further affect. Set R206 just to the point of minimum recovery time.

11. Scope probe on collector of Q50. Adjust R232 counterclockwise. Recovery time after the trailing edge will decrease to about 1 microsecond. Beyond this point adjustment has no further affect. Set R232 just to the point of minimum recovery time.

3.4.5 Pulse-Width Discrimination Circuitry Adjustment

The pulse-width discrimination adjustment shall be performed as follows:

1. With a large signal still applied to the input (step 9 of section 3.4.4) and scope probe on base of Q52, adjust R215 for minimum delay line reflection.

2. Accurately measure the noise level at the emitter of Q52. The level at the emitter of Q51 should be set to the same level by adjustment of R223.

3. The location of the delay line tap is determined by trial and error. The proper location of the tap is the point which gives maximum signal-to-noise ratio for a target. Since the transmitter pulse length and shape cannot be accurately duplicated, the best procedure is to aim the antenna at a fixed point target and move the tap until the point of maximum output is located.

3.4.6 Video Output Circuitry Adjustment

The video output adjustments should be set for the best indicator presentation. The controls are R240 for video gain, R242 for baseline clipping, and R246 for limit level.

3.4.7 Normal Receiver Adjustment

The normal receiver adjustment shall be performed as follows:

1. The IF alignment for the normal receiver output requires no additional tuning since the same IF strip is used for the normal and linear circuits.

2. Video circuit adjustments are set for best presentation on the indicator. The controls are R260 for video gain and R267 for limit level.

NOTE

Although all four channels contribute some noise to the adder regardless of the input noise amplitude, there is one predominant contributor for any given noise level. The following table shows the range over which each channel contributes a major portion of the noise. For example, if, in varying over the 60-DB range, the noise level increases at about 40 DB above MDS, output from channel 3 should be reduced. That is, R113 should be varied for the leading edge side, or R128 for the trailing edge side. However, if the noise level is low at about 40 DB, the other three channels should be slightly reduced.

Table 1. CFAR Video Channel Ranges

Noise Level (DB above MDS)	0-15	15-30	30-45	45-60
Primary Contributor	Channel 1	Channel 2	Channel 3	Channel 4
Adjustment for Leading Edge Side	R 185	R 147	R 113	R 73
Adjustment for Trailing Edge Side	R 200	R 164	R 128	R 96

3.5 SYSTEM CHECK

3.5.1 Linearity Check

The linearity check shall be performed as follows:

1. Apply a 30-MC signal to the input of the preamplifier.
2. Decrease the signal to the smallest discernible signal.

3. Switch the generator to "CW" output. Increase the level gradually to about 60 DB larger than the original setting.

4. If the noise level remains essentially constant over this range, the linear receiver portion of the receiver is operating properly. If not, refer to section 3.4.3 of the alignment procedure.

3.5.2 CFAR Check

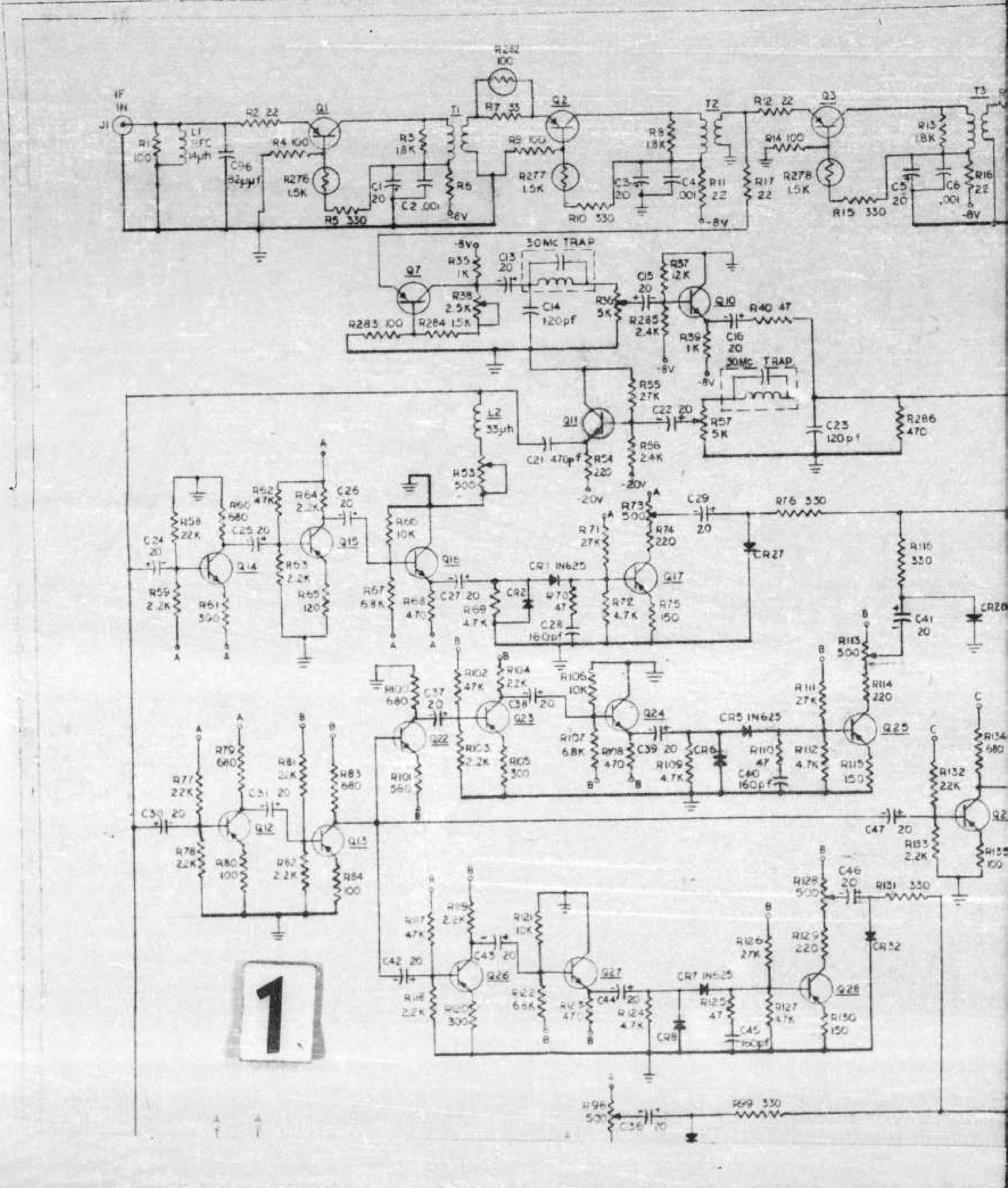
The CFAR check shall be performed as follows:

1. Vary the preamplifier bias. The noise level at the output should reach a maximum and then not increase further. (The character of the noise may change.)

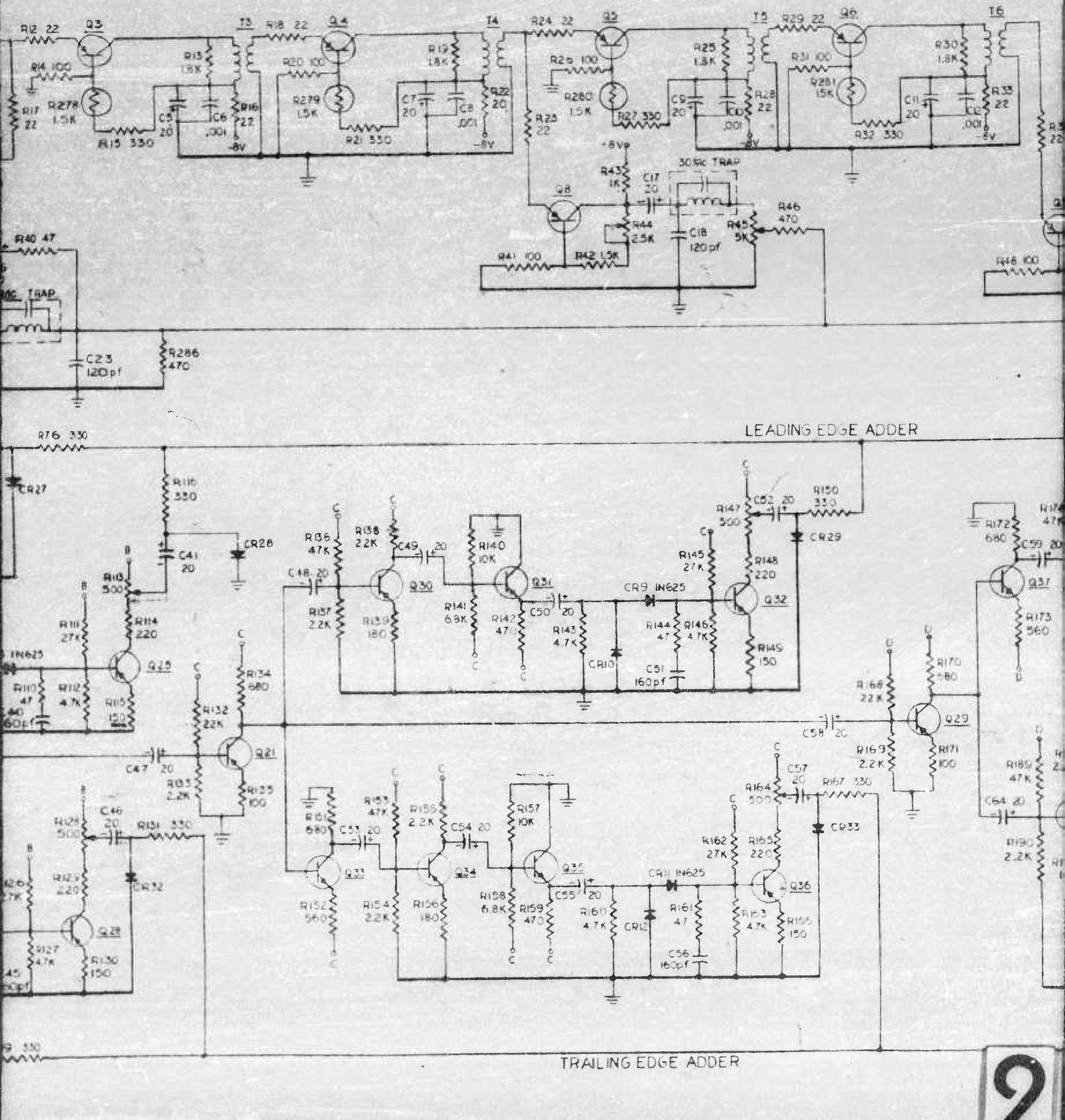
2. If this is so, the CFAR section is operating properly. Set the preamplifier bias at the point where the noise just reaches maximum.

3. If the noise level continues to increase, set resistors R206 and R232 to maximum counterclockwise and follow steps 2 through 11 in section 3.4.4 (video CFAR adjustment).

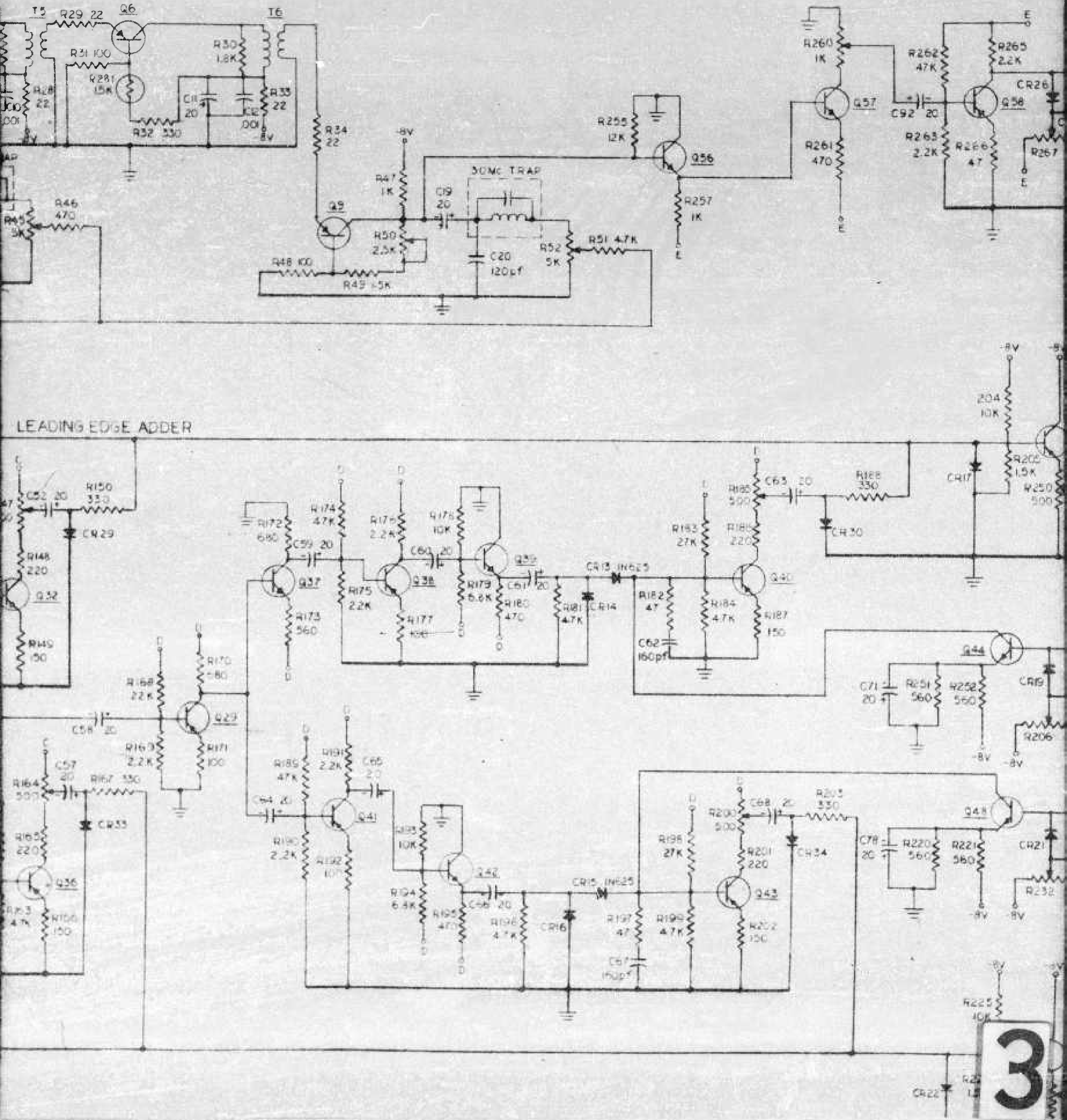
Figure 6. ATC LINAR Receiver, Schematic Diagram



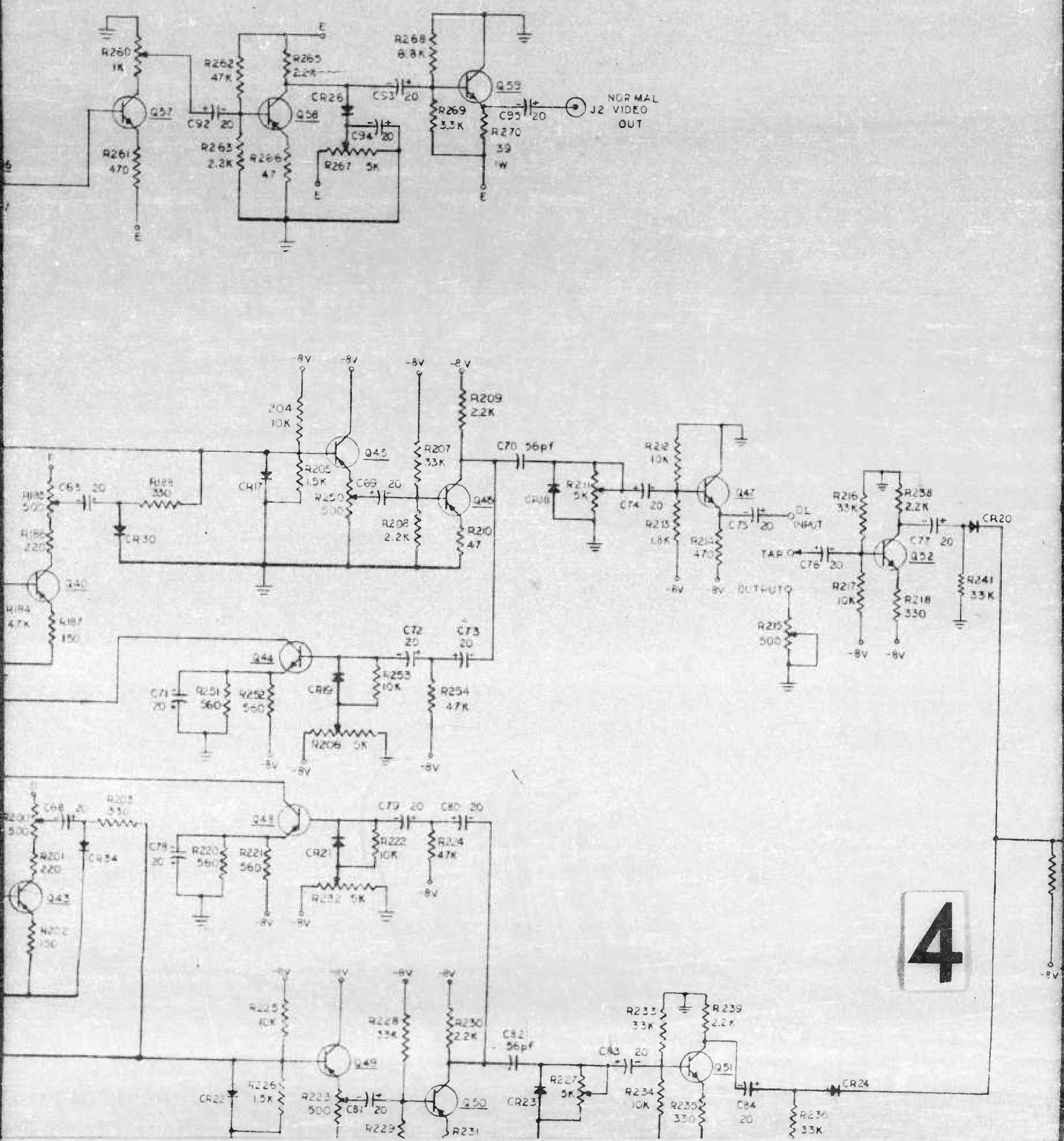
IF IN
J1
R1 100
L1 RFC 14μh
C96 82μμf
R2 22
R4 100
Q1
R276 1.5K
R5 330
C1 20
C2 .001
R3 1.8K
T1
R6
-8V
R282 100
R7 33
Q2
R9 100
R277 1.5K
R10 330
C3 20
R8 1.8K
C4 .001
R11 22
T2
-8V
R12 22
R17 22
Q3
R14 100
R278 1.5K
R15 330
R13 1.8K
C5 20
C6 .001
R16 22
T3
30MC TRAP
-8V
R35 1K
C13 20
Q7
R38 2.5K
R283 100
R284 1.5K
C14 120pf
R36 5K
C15 20
R37 12K
R285 2.4K
Q10
R40 47
C16 20
R39 1K
30Mc TRAP
L2 33μh
C21 470pf
R53 500
Q11
R54 220
-20V
R55 27K
R56 2.4K
C22 20
R57 5K
C23 120pf
R286 470
C24 20
R58 22K
R59 2.2K
Q14
R60 680
R61 390
C25 20
R62 47K
R63 2.2K
R64 2.2K
C26 20
Q15
R65 120
R66 10K
Q16
R67 6.8K
R68 470
C27 20
R69 4.7K
CR2
CR1 1N625
R70 47
C28 160pf
R71 27K
R72 4.7K
R73 500
R74 220
Q17
R75 150
C29 20
R76 330
CR27
R116 330
C41 20
CR28
R113 500
R114 220
Q25
R115 150
R100 680
C37 20
Q22
R101 560
R102 47K
R103 2.2K
R104 2.2K
C38 20
Q23
R105 300
R106 10K
R107 6.8K
R108 470
Q24
C39 20
R109 4.7K
CR6
CR5 1N625
R110 47
C40 160pf
R111 27K
R112 4.7K
R77 22K
R78 22K
C30 20
Q12
R79 680
R80 100
C31 20
R81 22K
R82 2.2K
Q13
R83 680
R84 100
C47 20
R132 22K
R133 2.2K
R134 680
R135 100
R117 47K
R118 2.2K
C42 20
Q26
R119 2.2K
C43 20
R120 300
R121 10K
R122 6.8K
Q27
R123 470
C44 20
R124 4.7K
CR8
CR7 1N625
R125 47
C45 160pf
R126 27K
R127 4.7K
R128 500
C46 20
R129 220
R131 330
CR32
Q28
R130 150
R96 500
C36 20
R99 330
1


LEADING EDGE ADDER
TRAILING EDGE ADDER
Q3
Q4
Q5
Q6
Q8
Q21
Q25
Q28
Q29
Q30
Q31
Q32
Q33
Q34
Q35
Q36
Q37
T3
T4
T5
T6
R12 22
R14 100
R278 1.5K
R15 330
R13 1.8K
R16 22
C5 20
C6 .001
R17 22
R18 22
R20 100
R279 1.5K
R21 330
R19 1.8K
C7 20
C8 .001
R22 20
-8V
R24 22
R26 100
R280 1.5K
R27 330
R23 22
R25 1.8K
C9 20
C10 .001
R28 22
R29 22
R31 100
R281 1.5K
R32 330
R30 1.8K
C11 20
C12 .001
R33 22
+8V
R43 1K
C17 20
30kc TRAP
R44 2.5K
R41 100
R42 1.5K
C18 120pf
R45 5K
R46 470
R48 100
R40 47
TRAP
C23 120pf
R286 470
R76 330
CR27
R116 330
C41 20
CR28
R113 500
R114 220
R111 27K
R112 4.7K
R110 47
R115 150
IN625
R132 22K
R134 680
R133 2.2K
R135 100
C47 20
R128 500
C46 20
R131 330
CR32
R129 220
R126 27K
R127 4.7K
R130 150
R136 47K
C48 20
R137 2.2K
R138 2.2K
C49 20
R139 180
R140 10K
R141 6.8K
R142 470
C50 20
R143 4.7K
CR10
CR9 IN625
R144 47
R146 4.7K
C51 160pf
R145 27K
R147 500
C52 20
R148 220
R149 150
R150 330
CR29
R172 680
C59 20
R173 560
R168 22K
R170 680
C58 20
R169 2.2K
R171 100
R189 47K
C64 20
R190 2.2K
R151 680
C53 20
R152 560
R153 47K
R154 2.2K
R155 2.2K
C54 20
R156 180
R157 10K
R158 6.8K
R159 470
C55 20
R160 4.7K
CR12
CR11 IN625
R161 47
C56 160pf
R162 27K
R163 4.7K
R164 500
C57 20
R165 220
R166 150
R167 330
CR33
B
C
D

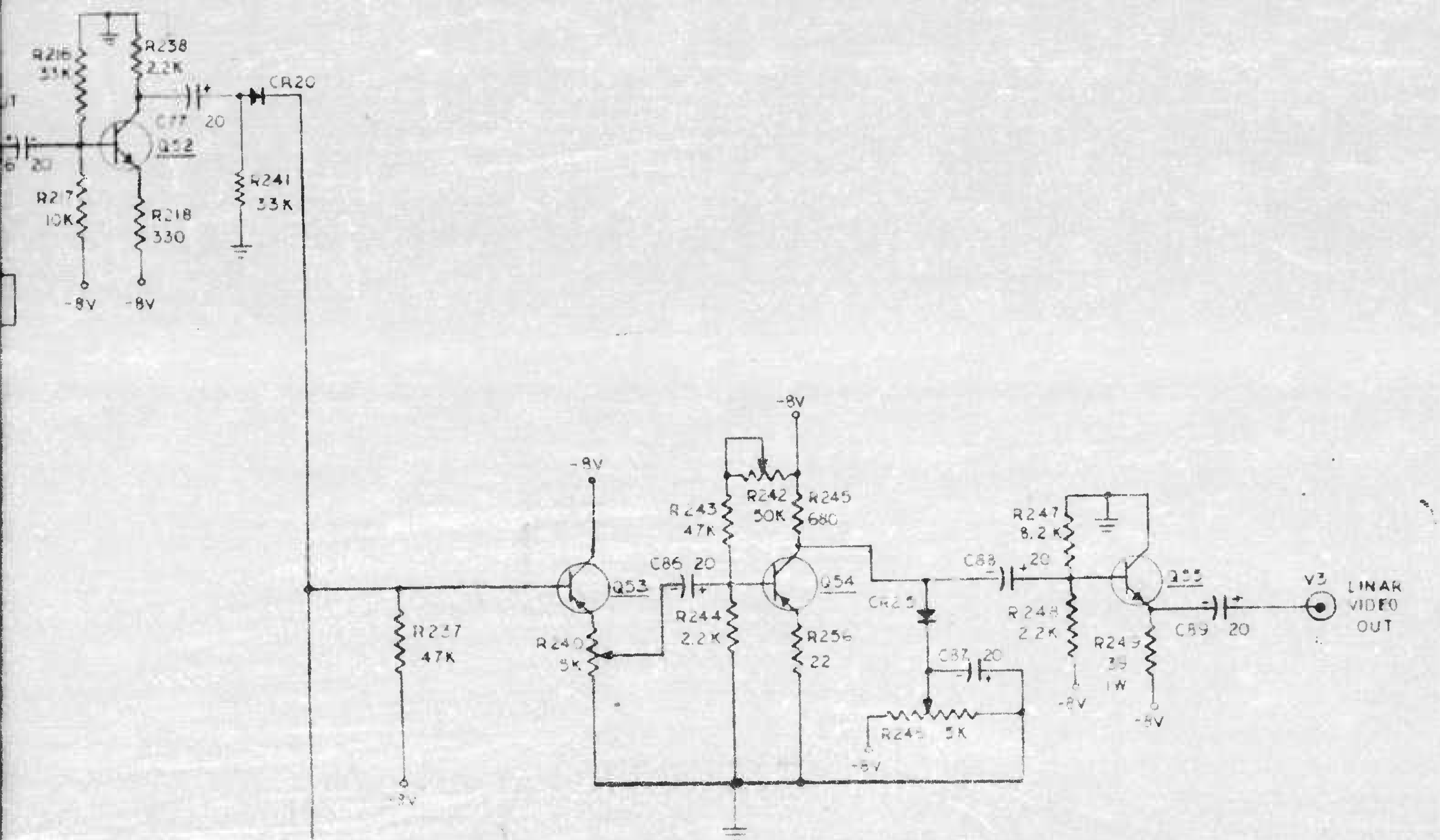
2



T5
R29 22
Q6
R31 100
R281 15K
R28 22
R32 330
R30 1.8K
C11 20
C12 .001
T6
R33 22
-8V
R34 22
Q9
R46 470
R45 5K
R48 100
R49 1.5K
R47 1K
R50 2.5K
C19 20
30MC TRAP
C20 120pf
R52 5K
R51 4.7K
R255 12K
Q56
R257 1K
R260 1K
Q57
R261 470
C92 20
R262 47K
R263 2.2K
R265 2.2K
Q58
R266 47
CR26
R267
LEADING EDGE ADDER
C52 20
R150 330
CR29
R148 220
Q32
R149 150
R172 680
C59 20
Q37
R173 560
R174 47K
R175 2.2K
R176 2.2K
C60 20
Q38
R177 100
R178 10K
R179 6.8K
Q39
C61 20
R180 470
R181 4.7K
CR14
CR13 IN625
R182 47
C62 160pf
R183 27K
R184 4.7K
R185 500
C63 20
R186 220
Q40
R187 150
R188 330
CR30
CR17
204 10K
R205 1.5K
R250 500
Q44
C71 20
R251 560
R252 560
CR19
R206
R168 22K
R169 2.2K
Q29
R170 680
R171 100
C58 20
R164 500
C57 20
R167 330
CR33
R165 220
Q36
R163 4.7K
R166 150
R189 47K
R190 2.2K
C64 20
Q41
R191 2.2K
C65 20
R192 100
R193 10K
R194 6.8K
Q42
R195 470
C66 20
R196 4.7K
CR16
CR15 IN625
R197 47
C67 150pf
R198 27K
R199 4.7K
R200 500
C68 20
R201 220
Q43
R202 150
R203 330
CR34
C78 20
R220 560
R221 560
Q48
CR21
R232
R225 10K
CR22
3



R260 1K
Q57
R261 470
C92 20
R262 47K
R263 2.2K
Q58
R265 2.2K
R266 47
CR26
C93 20
C94 20
R267 5K
R268 8.8K
R269 3.3K
Q59
R270 39 1W
C95 20
J2 NORMAL VIDEO OUT
204 10K
R205 1.5K
Q45
R207 33K
R208 2.2K
R209 2.2K
Q46
R210 47
R250 500
C69 20
C70 56pf
CR17
CR18
R211 5K
C74 20
R212 10K
R213 1.8K
Q47
R214 470
C75 20
DL INPUT
R215 500
TAP 0
C76 20
R216 33K
R217 10K
Q52
R218 330
R238 2.2K
C77 20
CR20
R241 33K
R185 500
C63 20
R128 330
CR30
R186 220
Q40
R184 4.7K
R187 150
Q44
C72 20
C73 20
C71 20
R251 560
R252 560
CR19
R253 10K
R254 47K
R206 5K
R200 500
C68 20
R203 330
CR34
R201 220
Q43
R202 150
Q48
C78 20
R220 560
R221 560
CR21
R222 10K
R224 47K
R232 5K
C79 20
C80 20
R225 10K
R226 1.5K
CR22
Q49
R223 500
C81 20
R228 33K
R229
R230 2.2K
Q50
R231
C82 56pf
CR23
R227 5K
C83 20
R233 33K
R234 10K
Q51
R235 330
R239 2.2K
C84 20
R236 33K
CR24
-8V
E
4



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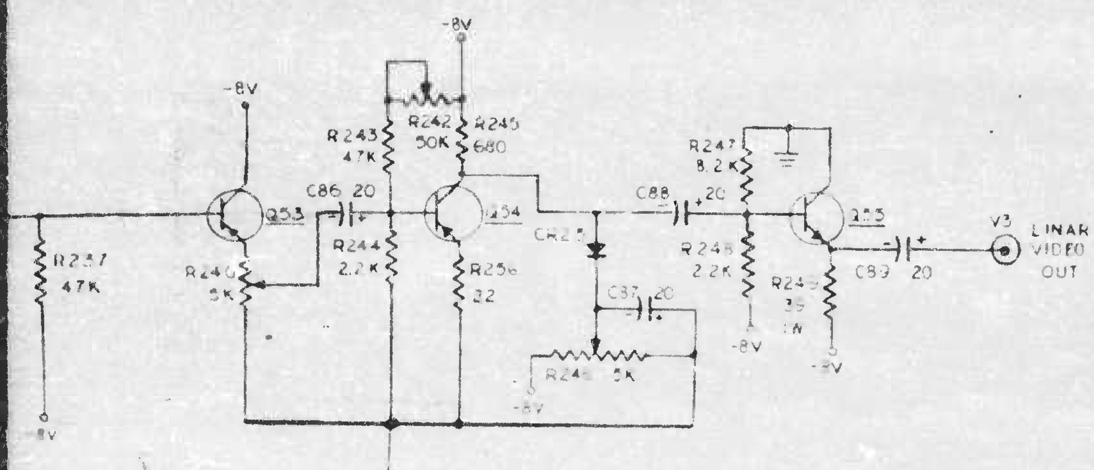
NOTES:

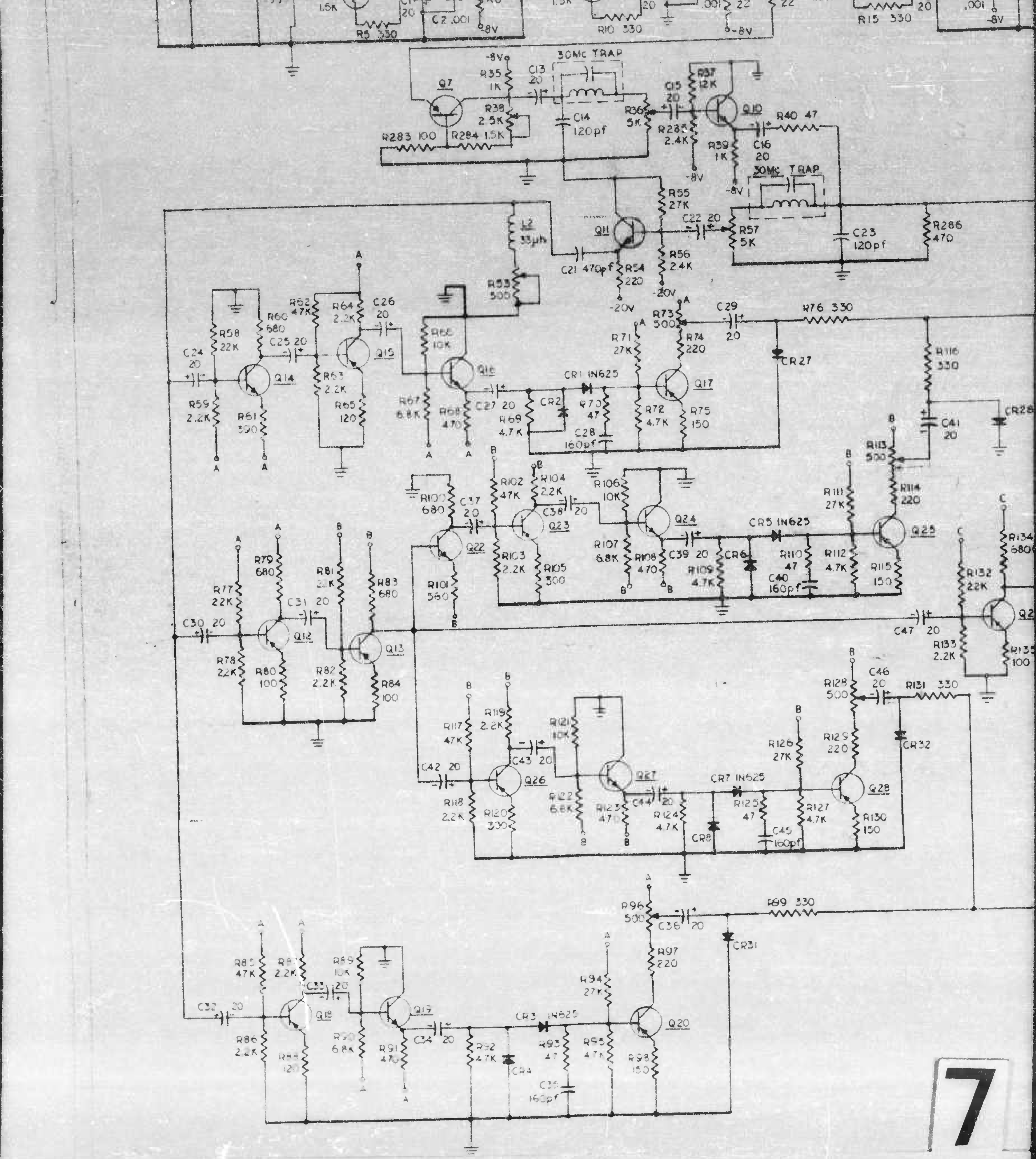
1-ALL PNP TRANSISTORS ARE TYPE 2N501/18.
2-ALL NPN TRANSISTORS ARE TYPE 2N706.
3-ALL CAPACITANCE IN MFD UNLESS OTHERWIS
4-ALL DIODES ARE TYPE IN116 UNLESS OTHERWI
5-R276 THRU R282 ARE TEMPERATURE VARIA
VALVES SHOWN ARE FOR 25°C.

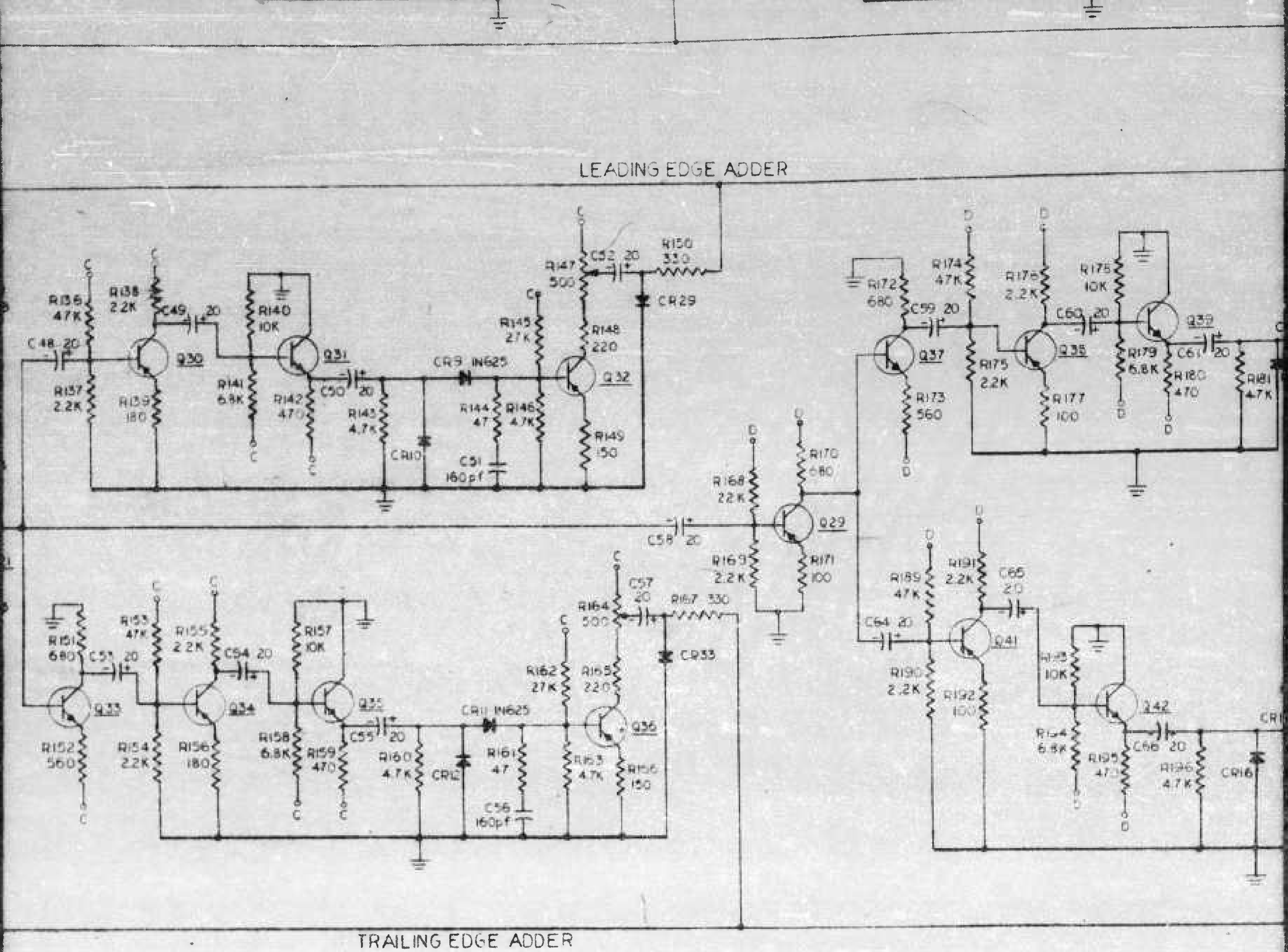


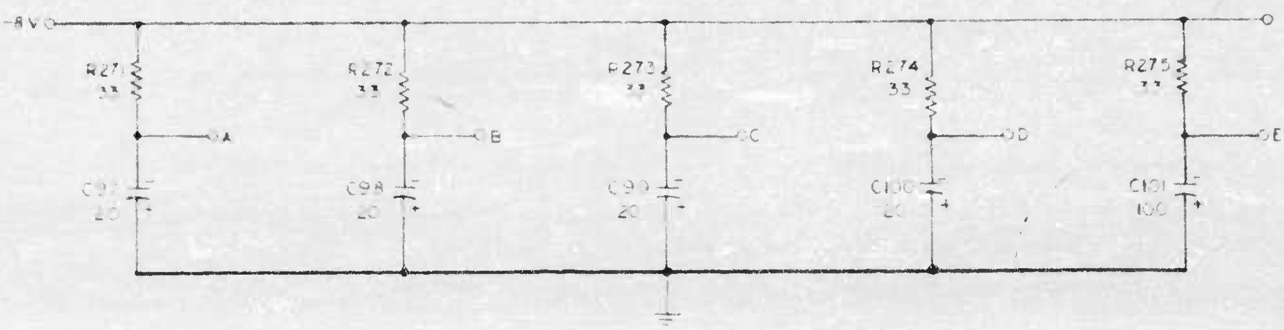
6

NOTES:

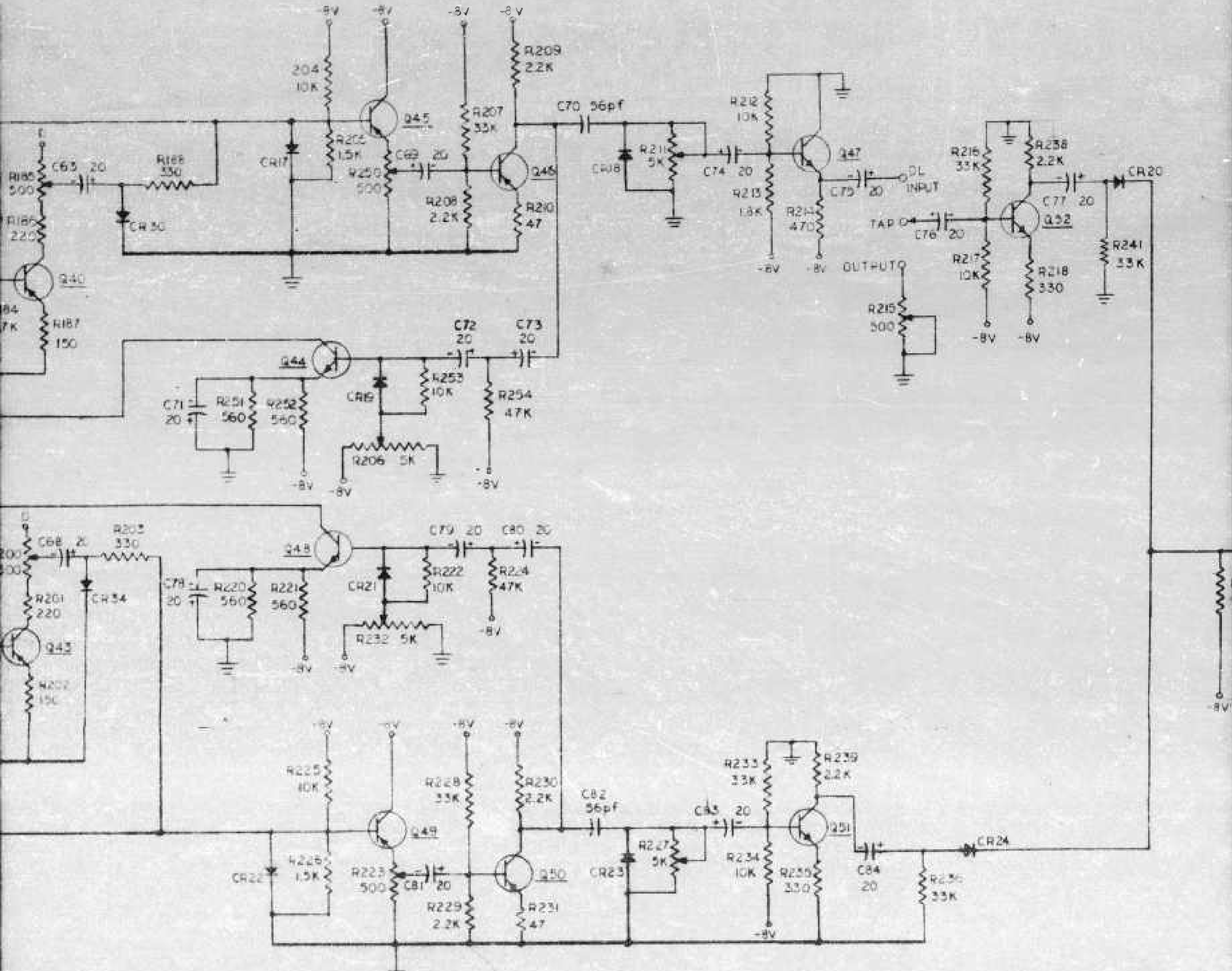
1. ALL PNP TRANSISTORS ARE TYPE 2N501/18.
2. ALL NPN TRANSISTORS ARE TYPE 2N706.
3. ALL CAPACITANCE IN MFD UNLESS OTHERWISE NOTED.
4. ALL DIODES ARE TYPE IN116 UNLESS OTHERWISE NOTED.
5. R276 THRU R282 ARE TEMPERATURE VARIABLE RESISTORS VALVES SHOWN ARE FOR 25°C.


R5 330
C2 .001
-8V
R10 330
.001
22
R15 330
-8V
Q7
R35 1K
C13 20
30Mc TRAP
C14 120pf
R38 2.5K
R283 100
R284 1.5K
R36 5K
C15 20
R37 12K
Q10
R285 2.4K
R40 47
R39 1K
C16 20
-8V
Q11
R55 27K
C22 20
R57 5K
30Mc TRAP
C23 120pf
R286 470
R56 2.4K
C21 470pf
R54 220
-20V
L2 33μh
R53 500
R58 22K
R60 680
C24 20
C25 20
Q14
R59 2.2K
R61 390
R62 47K
R64 2.2K
C26 20
Q15
R63 2.2K
R65 120
R66 10K
Q16
R67 6.8K
R68 470
C27 20
R69 4.7K
CR2
CR1 IN625
R70 47
C28 160pf
R71 27K
R73 500
R74 220
C29 20
R76 330
CR27
Q17
R72 4.7K
R75 150
R116 330
C41 20
CR28
R113 500
R114 220
R111 27K
Q25
R112 4.7K
R115 150
R100 680
C37 20
R102 47K
R104 2.2K
C38 20
Q23
Q22
R101 560
R103 2.2K
R105 300
R106 10K
Q24
R107 6.8K
R108 470
C39 20
CR6
R109 4.7K
CR5 IN625
R110 47
C40 160pf
R79 680
R77 22K
C31 20
Q12
R81 22K
R83 680
Q13
C30 20
R78 2.2K
R80 100
R82 2.2K
R84 100
R132 22K
R134 680
C47 20
R133 2.2K
R135 100
R117 47K
R119 2.2K
C43 20
R121 10K
Q27
C42 20
Q26
R118 2.2K
R120 330
R122 6.8K
R123 470
C44 20
R124 4.7K
CR8
CR7 IN625
R125 47
C45 160pf
R126 27K
R127 4.7K
Q28
R128 500
C46 20
R131 330
CR32
R129 220
R130 150
R96 500
C36 20
R99 330
CR31
R97 220
R94 27K
Q20
R98 150
R85 47K
R87 2.2K
C33 20
R89 10K
Q18
Q19
C32 20
R86 2.2K
R88 120
R90 6.8K
R91 470
C34 20
R92 4.7K
CR4
CR3 IN625
R93 47
C35 160pf
R95 4.7K


LEADING EDGE ADDER
TRAILING EDGE ADDER
Q29
Q30
Q31
Q32
Q33
Q34
Q35
Q36
Q37
Q38
Q39
Q41
Q42
CR9 IN625
CR10
CR11 IN625
CR12
CR29
CR33
C51 160pf
C56 160pf
R147 500
R150 330
R164 500
R167 330

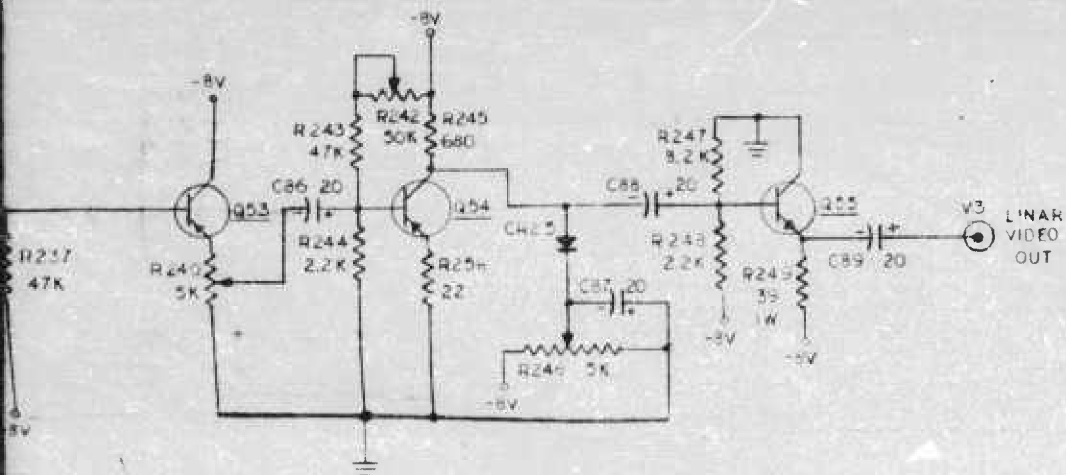

-8V
R271 33
R272 33
R273 33
R274 33
R275 33
A
B
C
D
E
C97 20
C98 20
C99 20
C100 20
C101 100

8



-8V
R209 2.2K
204 10K
Q45
R207 33K
C70 56pf
R212 10K
Q47
R238 2.2K
R216 33K
CR20
R205 1.5K
C69 20
R250 500
Q46
CR17
CR18
R211 5K
C74 20
R213 1.8K
R214 470
C75 20
DL INPUT
C77 20
Q52
TAP
C76 20
R217 10K
R218 330
R241 33K
OUTPUT
R215 500
R185 500
C63 20
R188 330
R186 220
CR30
R208 2.2K
R210 47
Q40
R187 150
C72 20
C73 20
Q44
R253 10K
R254 47K
C71 20
R251 560
R252 560
CR19
R206 5K
C68 20
R203 330
C79 20
C80 20
Q48
R222 10K
R224 47K
C78 20
R220 560
R221 560
CR21
CR34
R201 220
R232 5K
Q43
R202 150
R225 10K
R228 33K
R230 2.2K
C82 56pf
C83 20
R233 33K
R239 2.2K
Q49
Q50
Q51
R226 1.5K
R223 500
C81 20
CR22
CR23
R227 5K
R234 10K
R235 330
C84 20
CR24
R236 33K
R229 2.2K
R231 47

9



NOTES:

1-ALL PNP TRANSISTORS ARE TYPE 2N501/18.
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3-ALL CAPACITANCE IN MFD UNLESS OTHERWISE NOTED.
4-ALL DIODES ARE TYPE 1N116 UNLESS OTHERWISE NOTED.
5-R276 THRU R282 ARE TEMPERATURE VARIABLE RESISTORS. VALVES SHOWN ARE FOR 25°C.

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NEXT ASSY / USED ON / APPLICATION	SCHEMATIC DIAGRAM BENDIX ATC LINAR RECEIVER	THE Bendix CORPORATION BENDIX RADIO DIVISION BALTIMORE 4, MARYLAND N16400